REMARKS

This AMENDMENT UNDER 37 CFR 1.111 is filed in reply to the outstanding Office Action of July 21, 2004, and is believed to be fully responsive thereto and to place this case in condition for allowance for reasons set forth below in greater detail.

Reconsideration is respectfully requested of the rejection of claims 1-4 as being allegedly obvious over Faucon et al in view of Datta et al, particularly in view of the clarifying amendments to each of independent claims 1, 3 and 4 and the following comments on the distinctions of each of the present invention over the applied prior art of Faucon et al and Datta et al.

The Present Invention

The problem that the present invention seeks to solve is to allow a high speed master high performance processor to access a high latency memory without stalling the processor. The solution is to use a low speed slave processor to access the memory, freeing the master processor to continue other processing operations and tasks while the slave processor accesses the memory to allow the slave processor to absorb any latency or waiting associated with execution of the read command. The slave processor then posts the results of the reads to the master processor later.

Faucon et al

In summary, Faucon et al. suffers from the very problem which the present invention is designed to solve, namely the DSP of Faucon is stalled, suffering the full consequences of any latency or waiting while a memory read/write operation is being performed with the assistance of a data transfer element in Faucon.

Faucon recognises challenges in a system design which are similar to the challenges recognized by the present invention, as discussed in their background. But the form of their solution is quite different, in that Faucon provides a data transfer element that can pipeline (provide multiple consecutive accesses in sequence) data transfers, and are able to access

multiple closely placed addresses by using an offset register to describe the offset for each consecutive transfer. This provides the advantage that the offsets can be encoded in smaller instructions with less memory cost, which reduces the memory throughput needed for the instructions as a whole.

But the DSP is still stalled and blocked waiting for the first memory access to be returned. The action of the memory controller does not reduce the time for the first memory access, but it optimizes subsequent nearby memory accesses, which can be reached by the offset register.

In the present invention the master processor continues other tasks while the slave processor performs the access to memory and returns the results. This makes it appropriate where the latency for memory access is many cycles, maybe the time for hundreds of local memory accesses.

If only a single memory access is required, then Faucon provides no advantage, whereas the present invention provides a distinct advantage if the memory access delay is very large.

This is essentially a similar distinction to that of previously applied Platko.

Faucon provides a system that addresses the limitation on digital signal processor (DSP) system performance by reducing the number of clock cycles required to transfer data between internal and external memory. Faucon reduces the size of the instruction set, thereby reducing the size of the memory and thus also reducing the overall size of the DSP system.

Faucon transfers data in a single clock cycle between a digital signal processor (DSP) core and a memory unit. The system includes a data transfer element coupled between the memory unit and the DSP core, where the data transfer element is adapted to transfer the data between the memory unit and the DSP core in a single clock cycle clock cycle. Faucon functions

by pipelining the data from the memory unit to the DSP core in a single clock cycle after the pipeline has been primed.

In one embodiment, the data transfer element is a coprocessor including a plurality of latch devices coupled between the DSP core and the external memory unit via a plurality of data buses, respectively. The latch devices provide intermediate registers in the coprocessor for storing the data being transferred between the DSP core and the external memory. Data are transferred into the coprocessor during a first clock cycle and out of the coprocessor in a second clock cycle immediately following the first clock cycle. column 2, lines 14-44

A key difference of the present invention is that the master processor is able to continue processing operations while the read is being performed by the slave processor.

Those features of the present invention are mentioned in the specification at page 8, lines 12-13, "In the meantime the processor is free to perform other tasks," and at page 11, lines 15-21, "Advantageously, the master processor 10 does not then have to wait or otherwise stall until the requested data is returned from the memory 50. This is because the master processor 10 has effectively delegated execution of the read request to the slave processor 20. The slave processor 30 absorbs any waiting, stalling or other latency associated with the memory access."

Datta et al

In summary, Datta et al. merely discloses a well known data processing concept of task off-loading, and does not disclose or teach off-loading a single memory access to a different processor.

Datta was apparently cited to prove that the concept is well known of using a master-slave configuration, where the master is able to offload a task and continue processing while the slave carries on 'simultaneously performing the offloaded task'.

Task offload is well-known in data processing. However, what is not well-known, is that a single memory access (for example) can be offloaded to a different processor.

None of the prior art memory controllers disclose or teach this feature.

This application is now believed to be in condition for allowance, a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

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